

## **Chapter 2: Introduction to the AVR Microcontroller**

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### **TRUE/FALSE**

1. Mega AVR devices have from 32 to 384 kB of memory.

ANS: F                      PTS: 1

REF: 2.2 An Overview of the AVR Microcontroller Family

2. The V bit (Two's Complement Overflow flag) of the status register indicates whether an overflow occurs in the previous operation.

ANS: T                      PTS: 1

REF: 2.4 The AVR CPU Register

3. Direct Data Addressing Mode uses the contents of one of the pointers (X, Y, or Z) to specify the address of the data memory location to access.

ANS: F                      PTS: 1

REF: 2.6 AVR Addressing Modes

4. The arithmetic and logic instructions of the AVR cannot use memory locations as their operand. The value stored in a memory location must be copied to a register before it can be operated on.

ANS: T                      PTS: 1

REF: 2.7 A Sample of AVR Instructions

5. The AVR has a version of the SUB instruction that can be used to perform multiprecision subtraction operations.

ANS: T                      PTS: 1

REF: 2.8 Summary

### **COMPLETION**

1. An AVR instruction can be divided into two parts: the \_\_\_\_\_ and \_\_\_\_\_ fields.

ANS:  
opcode operand  
operand opcode

PTS: 1

REF: 2.5 The AVR Instruction Set

2. The ELPM instruction uses the Z pointer to specify the program memory location to access. When the ELPM instruction is used, the \_\_\_\_\_ register is used to extend the Z pointer.

ANS: RAMPZ

PTS: 1

REF: 2.6 AVR Addressing Modes

3. The subtraction instruction that subtracts the constant k ( $0 \leq k \leq 63$ ) from the register pair Rd+1:Rd and places the difference in Rd+1:Rd (Rd is 24, 26, 28, or 30) is called \_\_\_\_\_.

ANS:  
sbiw Rd, k

subtract immediate from word

PTS: 1 REF: 2.7 A Sample of AVR Instructions

4. The lpm (load program memory) instruction loads the contents of the program memory location pointed to by Z to register \_\_\_\_\_.

ANS: r0

PTS: 1 REF: 2.7 A Sample of AVR Instructions

5. The 8-bit AVR microcontroller has a total of \_\_\_\_\_ CPU registers.

ANS: 32

PTS: 1 REF: 2.8 Summary

### SHORT ANSWER

1. Briefly describe the memory size, the number of instructions supported, and the maximum clock frequencies of the Mega and X Mega devices.

ANS:

The Mega devices have from 4 to 256 kB of program flash memory, support most of the AVR instructions (130-135), and have a maximum clock frequency of 20 MHz. The X Mega devices have from 32 to 384 kB of memory, implement all 142 instructions, and may run at a clock with a frequency as high as 32 MHz.

PTS: 1 REF: 2.2 An Overview of the AVR Microcontroller Family

2. Name four of the bits in the status register (SREG) and describe their functions.

ANS:

1. The Global Interrupt Enable Flag (I). This flag must be set to 1 in order for each individual interrupt source to be enabled. When it is cleared to 0, none of the individual interrupt sources are enabled.
2. Bit Copy Storage (T). This flag is used by the bit load and bit store instruction as the source or destination operand bit.
3. Half Carry Flag (H). The half carry flag indicates a half carry in some arithmetic operations.
4. Sign bit (S). This flag indicates the sign of the previous operation result and is always the exclusive OR of the N and V flags.
5. Two's Complement Overflow Flag (V). This flag indicates whether an overflow occurs in the previous operation.
6. Negative flag (N). This flag indicates whether the previous arithmetic or logical operation is negative.
7. Zero Flag (Z). This flag indicates whether the previous arithmetic or logical operation result is zero.
8. Carry Flag (C). This flag indicates whether a carry is generated in the previous arithmetic or logical operation.

PTS: 1 REF: 2.4 The AVR CPU Register

3. Briefly describe the function of the RAMPD register.

ANS:

The XMega AVR devices provide this register to support direct addressing of the whole data memory space above 64 kB. This register is concatenated with the k operand in the instruction. The content of this register and the k field in the instruction are used as the direct address to access data memory.

PTS: 1 REF: 2.4 The AVR CPU Register

4. Some complex AVR devices have more peripheral registers than can be supported within the 64 locations reserved in the instruction for I/O direct addressing. How can this extended I/O memory be accessed?

ANS:

The extended I/O memory can only be reached by using the data memory addressing. I/O registers in the extended I/O memory space must be accessed using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

PTS: 1 REF: 2.6 AVR Addressing Modes

5. Name three AVR addition instructions described in this chapter and give a brief description of each.

ANS:

1. add Rd, Rr. (Add without carry) This instruction add the contents of registers Rd and Rr and places the sum in Rd.

2. adc Rd, Rr. (Add with carry) This instruction adds the values in Rd and Rr and the C flag of the SREG register, and places the sum in Rd.

3. adiw Rd, k. (Add immediate to word) This instruction adds the constant k (0-63) to the register pair Rd+1:Rd and places the sum in the register pair Rd+1:Rd. Here, Rd can only be 24, 26, 28, and 30.

PTS: 1 REF: 2.7 A Sample of AVR Instructions