Exercise Problems

3.1 Consider a MOS system with the following parameters:

$$t_{ox} = 1.6\text{nm}$$
$$\phi_{GC} = -1.04\text{V}$$
$$\text{N}_\text{A} = 2.8 \cdot 10^{18}\text{cm}^{-3}$$
$$Q_{OX} = q4 \cdot 10^{10}\,\text{C/cm}^2$$

a. Determine the threshold voltage V_{T0} under zero bias at room temperature (T = 300 K). Note that $\varepsilon_{ox} = 3.97\varepsilon_0$ and $\varepsilon_{si} = 11.7\varepsilon_0$.

SOLUTION :

First, calculate the Fermi potentials for the p-type substrate and for the n-type polysilicon gate:

$$\phi_F(substrate) = \frac{kT}{q}\ln\left(\frac{n_i}{N_A}\right) = 0.026\text{V} \cdot \ln\left(\frac{1.45 \cdot 10^{10}}{2.8 \times 10^{18}}\right) = -0.49\text{V}$$

The depletion region charge density at $V_{SB} = 0$ is found as follows:

$$\begin{aligned} Q_{B0} &= -\sqrt{2 \cdot q \cdot N_A \cdot \varepsilon_{Si} \cdot \left|-2\phi_F(substrate)\right|} \\ &= -\sqrt{2 \cdot 1.6 \cdot 10^{-19} \cdot (2.8 \times 10^{18}) \cdot 11.7 \cdot 8.85 \cdot 10^{-14} \cdot \left|-2 \cdot 0.49\right|} \\ &= -9.53 \cdot 10^{-7}\,\text{C/cm}^2 \end{aligned}$$

The oxide-interface charge is:

$$Q_{ox} = q \cdot N_{ox} = 1.6 \times 10^{-19}\text{C} \times 4 \cdot 10^{10}\text{cm}^{-2} = 6.4 \cdot 10^{-9}\,\text{C/cm}^2$$

The gate oxide capacitance per unit area is calculated using the dielectric constant of silicon dioxide and the oxide thickness t_{ox}.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97 \cdot 8.85 \cdot 10^{-14}\,\text{F/cm}}{1.6 \cdot 10^{-7}\,\text{cm}} = 2.2 \cdot 10^{-6}\,\text{F/cm}^2$$

Now, we can combine all components and calculate the threshold voltage.

$$\begin{aligned} V_{T0} &= \phi_{GC} - 2\phi_F(substrate) - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \\ &= -1.04 - (-0.98) - (-0.53) - (0.03) = 0.44\text{V} \end{aligned}$$

b. Determine the type (p-type or n-type) and amount of channel implant (N_I/cm^2) required to change the threshold voltage to 0.6V

SOLUTION :

p-type implanted needed in the amount of:

$$\Delta V = 0.6 - V_{T0} = 0.6 + 0.44 = 1.04 = \frac{qN_I}{C_{ox}}$$

$$N_I = \frac{1.04C_{ox}}{q} = \frac{1.04 \cdot 2.2 \times 10^{-6}}{1.6 \times 10^{-19}} = 1.43 \times 10^{13}\,\text{cm}^{-2}$$

3.2 Consider a diffusion area that has the dimensions $0.4\mu\text{m} \times 0.2\mu\text{m}$ and the abrupt junction depth is $32\,\text{nm}$. Its n-type impurity doping level is $N_D = 2 \cdot 10^{20}\text{cm}^{-3}$ and the surrounding p-type substrate doping level is $N_A = 2 \cdot 10^{20}\text{cm}^{-3}$. Determine the capacitance when the diffusion area is biased at 1.2V and substrate is biased at 0V. In this problem, assume that there is no channel-stop implant.

SOLUTION :

$$C_j(V) = A \cdot \sqrt{\frac{\varepsilon_{si} \cdot q}{2}\left(\frac{N_A \cdot N_D}{N_A + N_D}\right)} \cdot \frac{1}{\sqrt{\phi_0 - V}}$$

$$\phi_0 = \frac{kT}{q}\ln\frac{N_A \cdot N_D}{n_i^2} = 0.026\ln\frac{2 \times 10^{20} \cdot 2 \times 10^{20}}{(1.45 \times 10^{10})^2} = 1.21$$

$$A = \left[0.2 \times 0.4 + 2\left(0.2 \times 0.032\right) + 2\left(0.4 \times 0.032\right)\right] = 1.18 \times 10^{-9}[cm^2]$$

$$C_j(V) = 1.18 \times 10^{-9}\sqrt{\frac{11.7 \cdot 8.854 \times 10^{-14} \cdot 1.6 \times 10^{-19}}{2}\left(\frac{4 \times 10^{40}}{4 \times 10^{20}}\right)} \frac{1}{\sqrt{1.21 + 1.2}}$$

$$= 2.18 \times 10^{-15}[F]$$

3.3 Describe the relationship between the mask channel length, L_M, and the electrical channel length, L. Are they identical? If not, how would you express L in terms of L_M and other parameters?

SOLUTION :

The electrical channel length is related to the mask channel length by:

$$L = L_M - 2L_D$$

Where L_D is the lateral diffusion length.

3.4 How is the device junction temperature affected by the power dissipation of the chip and its package? Can you describe the relationship between the device junction temperature, ambient temperature, chip power dissipation and the packaging quality?

SOLUTION :

The device junction temperature at operating condition is given as $T_j = T_a + \Theta P_{diss}$, where T_a is the ambient temperature; P_{diss} is the power dissipated in the chip; Θ is the thermal resistance of the packaging. A cheap package will have high Θ which will result in large and possibly damaging junction temperature. Thus the choice of packaging must be such that it is both economic and pretective of the device.

3.5 Describe the three components of the load capacitance C_{load}, where a logic gate is driving other fanout gates.

SOLUTION :

The three major components of the load capacitance are interconnect capacitance, the next stage input capacitance, i.e., the gate capacitance and the drain parasitic capacitances of the current stage.

3.6 Consider a layout of an nMOS transistor shown in Fig. P3.6.
The process parameters are:

$$N_D = 2 \cdot 10^{20}\,\text{cm}^{-3}$$
$$N_A = 2 \cdot 10^{20}\,\text{cm}^{-3}$$
$$X_j = 32\text{nm}$$
$$L_D = 10\text{nm}$$
$$t_{ox} = 1.6\text{nm}$$
$$V_{T0} = 0.53\text{V}$$
$$\textit{Channel stop doping} = 16.0 \times (\textit{p} - \textit{type substrate doping})$$

Find the effective drain parasitic capacitance when the drain node voltage changes from 1.2V to 0.6V.

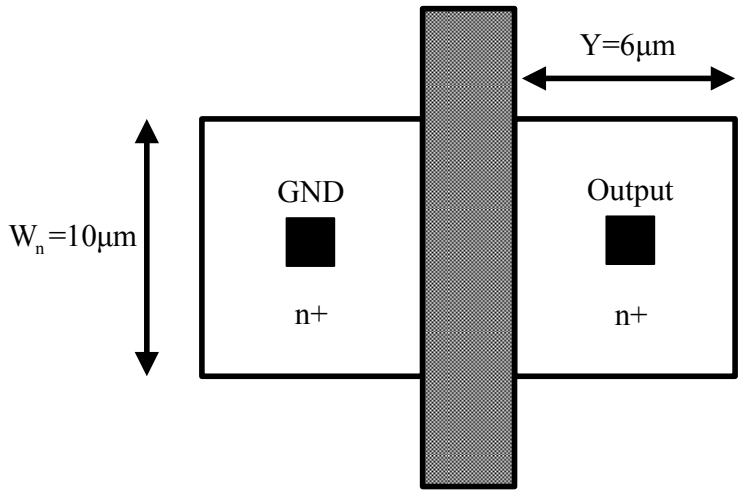


Figure P3.6

SOLUTION :

$$\phi_0 = \frac{kT}{q}\ln\frac{N_A \cdot N_D}{n_i^2} = 0.026\ln\left[\frac{2\times10^{20}\cdot 2\times10^{20}}{(1.45\times10^{10})^2}\right] = 1.21$$

$$\phi_{osw} = \frac{kT}{q}\ln\frac{N_A' \cdot N_D}{n_i^2} = 0.026\ln\left[\frac{16\times 2\times10^{20}\cdot 2\times10^{20}}{(1.45\times10^{10})^2}\right] = 2.31$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{si}\cdot q}{2}\left(\frac{N_A\cdot N_D}{N_A+N_D}\right)}\cdot\frac{1}{\sqrt{\phi_0}}$$

$$= \sqrt{\frac{11.7\times8.854\times10^{-14}\times1.6\times10^{-19}\times10^{20}}{2\times1.21}} = 2.61\times10^{-6}[\mathrm{F/cm^2}]$$

$$C_{josw} = \sqrt{\frac{\varepsilon_{si}\cdot q}{2}\left(\frac{N_A'\cdot N_D}{N_A'+N_D}\right)}\cdot\frac{1}{\sqrt{\phi_{osw}}}$$

$$= \sqrt{\frac{11.7\times8.854\times10^{-14}\times1.6\times10^{-19}\times1.88\times10^{20}}{2\times2.31}} = 2.59\times10^{-6}[\mathrm{F/cm^2}]$$

$$C_{jsw} = X_j C_{josw} = 32\times10^{-9}\times2.59\times10^{-6} = 0.083[\text{pF/cm}]$$

$$A = Y\times W = 6\times10 = 60[\mu m^2]$$

$$P = 2(Y+W) = 2(6+10) = 32[\mu m]$$

$$K_{eq} = 2\sqrt{\phi_0}\left(\frac{\sqrt{\phi_0+5}-\sqrt{\phi_0+2.5}}{5-2.5}\right)$$

$$= 2\sqrt{0.8967}\left(\frac{\sqrt{5.8967}-\sqrt{3.3967}}{2.5}\right) = 0.44$$

$$K_{eq}' = 2\sqrt{\phi_0}\left(\frac{\sqrt{\phi_0+5}-\sqrt{\phi_0+2.5}}{5-2.5}\right)$$

$$= 2\sqrt{0.8967}\left(\frac{\sqrt{5.8967}-\sqrt{3.3967}}{2.5}\right) = 0.44$$

$$C_{drain} = Keq\cdot Cj0\cdot A + Keq'\cdot Cjsw\cdot P$$
$$= 0.44\times9.6\times10^{-9}\times60\times10^{-8} + 0.46\times1.847\times10^{-12}\times32\times10^{-4}$$
$$= 5.25[\,fF\,]$$

3.7 A set of *I-V* characteristics for an nMOS transistor at room temperature is shown for different biasing conditions. Figure P3.7 shows the measurement setup.
Using the data, find : (a) the threshold voltage V_{T0} and, (b) velocity saturation v_{sat}.

Some of the parameters are given as: W=0.6μm, E_cL=0.4 V, λ=0.05, t_{ox} = 16 Å, $|2\phi_F|$ = 1.1 V.

V_{GS} (V)	V_{DS} (V)	V_{SB} (V)	I_D (μA)
0.6	0.6	0.0	6
0.65	0.6	0.0	12
0.9	1.2	0.3	44
1.2	1.2	0.3	156

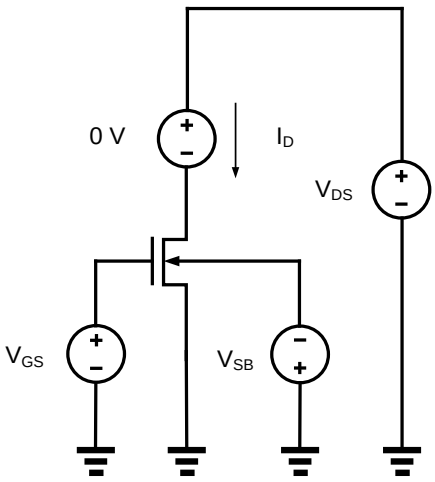


Figure P3.7

SOLUTION :

(a)

First, the MOS transistor is on ($I_D > 0$) for $V_{GS} > 0$ and $V_{DS} > 0$. Thus, the transistor must be an n-channel MOSFET. Assume that the transistor is enhancement-type and, therefore, operating mode.

$$I_D = W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(\mathrm{V}_{GS} - \mathrm{V}_T)^2}{(\mathrm{V}_{GS} - \mathrm{V}_T) + E_c L}(1 + \lambda \mathrm{V}_{DS})$$

When V_{GS} and V_T are similar, velocity saturation terms are neglected.

Let (V_{GS1}, I_{D1}) and (V_{GS2}, I_{D2}) be any two current-voltage pairs obtained from the table. Then, the V_{T0}, can be calculated.

$$\frac{I_{D1}}{I_{D2}} = \frac{(\mathrm{V}_{GS1} - \mathrm{V}_{T0})^2}{(\mathrm{V}_{GS2} - \mathrm{V}_{T0})^2} \Rightarrow V_{T0} = \frac{\sqrt{\frac{6\mu\mathrm{A}}{12\mu\mathrm{A}}} \times 0.65\mathrm{V} - 0.6\mathrm{V}}{\sqrt{\frac{6\mu\mathrm{A}}{12\mu\mathrm{A}}} - 1} = 0.48\mathrm{V}$$

(b)

Find velocity saturation

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{0.16 \times 10^{-8}} = 216 \times 10^{-4} \left[F / m\right]$$

$$I_D = W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(\mathrm{V}_{GS} - \mathrm{V}_T)^2}{(\mathrm{V}_{GS} - \mathrm{V}_T) + E_c L}(1 + \lambda \mathrm{V}_{DS})$$

$$12 = 0.6 \times 10^{-6} \times v_{sat} \times 216 \times 10^{-6} \times \frac{0.17^2}{0.17 + 0.4}(1 + 0.05 \times 0.6)$$

$$v_{sat} = 1.06 \times 10^6 \left[m / s\right]$$

3.8 Compare the two technology scaling methods, namely, (1) the constant electric field scaling and (2) the constant power supply voltage scaling. In particular, show analytically by using equations how the delay

time, power dissipation, and power density are affected in terms of the scaling factor, S. To be more specific, what would happen if the design rules change from, say, 1 μm to 1/S μm (S>1)?

SOLUTION :

	$Const.E-field$	$Const.V_{DD}$
W, L, t_{ox}	$1/S$	$1/S$
V_{DD}	$1/S$	1
C_{ox}	S	S
$C \propto C_{ox}WL$	$1/S$	$1/S$
k_n, k_p	S	S
I_{DD}	$1/S$	S
$t_{delay} \propto \frac{C\Delta V}{I_{DD}}$	$1/S$	$1/S^2$
$Power \propto I_{DD}V_{DD}$	$1/S^2$	S
$Power\ density\left(\frac{Power}{Area}\right)$	1	S^3

3.9 A pMOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D = 1\times10^{16}\,\text{cm}^{-3}$, gate doping density (n-type poly) of $N_D = 10^{20}\,\text{cm}^{-3}$, $Q_{ox}/q = 4\cdot10^{10}\,\text{cm}^{-2}$, and gate oxide thickness of $t_{ox} = 1.6nm$. Calculate the threshold voltage at room temperature for V_{SB}=0. Use $\varepsilon_{si} = 11.7\varepsilon_0$

SOLUTION :

$$\phi_F(substrate) = \frac{kT}{q}\ln\frac{N_{D,sub}}{n_i} = 0.026\ln\frac{1\times10^{16}}{1.45\times10^{10}} = 0.348[\text{V}]$$

$$\phi_F(gate) = \frac{kT}{q}\ln\frac{N_{D,poly}}{n_i} = 0.026\ln\frac{1\times10^{20}}{1.45\times10^{10}} = 0.587[\text{V}]$$

$$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate) = 0.348 - 0.587 = -0.239[\text{V}]$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\times8.85\times10^{-14}}{0.1\times10^{-4}} = 3.45\times10^{-8}[F/cm^2]$$

$$Q_{B0} = \sqrt{2qN_{D,sub}\varepsilon_{si}\left|2\phi_F\right|}$$
$$= \sqrt{2\times1.6\times10^{-19}\times10^{16}\times11.7\times8.85\times10^{-14}\times2\times0.348}$$
$$= 4.8\times10^{-8}[C/cm^2]$$

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$
$$= -0.239 - 2\times0.348 - \frac{4.8\times10^{-8}}{3.45\times10^{-8}} - \frac{4\times10^{10}\times1.6\times10^{-19}}{3.45\times10^{-8}}$$
$$= -2.51[\mathrm{V}]$$

3.10 Using the parameters given, calculate the current through two nMOS transistors in series (see Fig. P3.11), when the drain of the top transistor is tied to V_{DD}, the source of the bottom transistor is tied to $V_{SS} = 0$ and their gates are tied to V_{DD}. The substrate is also tied to $V_{SS} = 0$ V. Assume that $W/L = 10$ for both transistors and L=4μm.

$k' = 168\ \mu A/V^2$
$V_{T0} = 0.48$ V
$\gamma = 0.52\ V^{1/2}$
$|2\phi_F| = 1.01$ V

Hint : The solution requires several iterations, and the body effect on threshold voltage has to be taken into account. Start with the KCL equation.

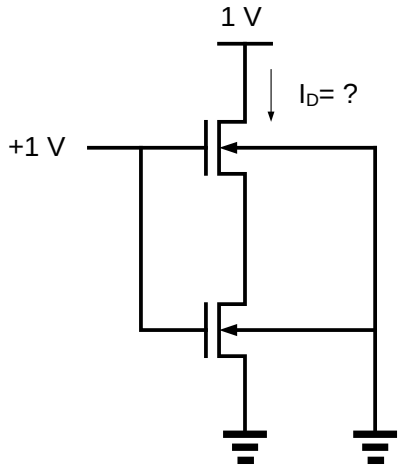


Figure P3.10

SOLUTION :

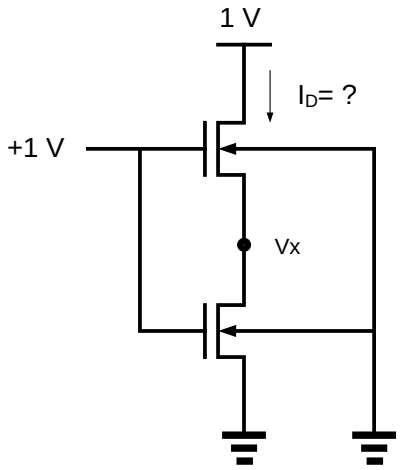


Figure P3.10

Since gate voltage is high, the midpoint V_x is expected to be low. Therefore, the load is in saturation and the driver is in linear region. From KCL

$$I_D = I_{D,driver} = I_{D,load}$$

$$\frac{1}{2}k'\frac{W}{L}\left(1-V_x-V_{T,L}(V_x)\right)^2 = \frac{1}{2}k'\frac{W}{L}\left(2\left(1-V_{T0}\right)V_x - V_x^{\,2}\right)$$

Using the following two equations to iterate find the solution.

$$\begin{cases}\left(1-V_x-V_{T,L}(V_x)\right)^2 = 1.04V_x - V_x^{\,2} \\ V_{T,L}(V_x) = 0.48 + 0.52\left(\sqrt{1.01+V_x} - \sqrt{1.01}\right)\end{cases}$$

The intermediate values are listed in the table:

$V_{T,L}(V_x)$	V_x
0.480	0.1523
0.518	0.1337
0.513	0.1359
0.514	0.1357
0.514	0.1357

$$I_D = \frac{1}{2}k'\frac{W}{L}(1.04V_x - V_x^{\,2}) = 0.5\times 168\times 10\times\left(1.04\times 0.1357 - 0.1357^2\right) = 103.1[\mu\text{A}]$$

3.11 The following parameters are given for an nMOS process:

t_{ox} = 16 Å
substrate doping $N_A = 4\cdot 10^{18}\,\text{cm}^{-3}$
polysilicon gate doping $N_D = 2\cdot 10^{20}\,\text{cm}^{-3}$
oxide-interface fixed-charge density $N_{ox} = 2\cdot 10^{10}\,\text{cm}^{-3}$

(a) Calculate V_T for an unimplanted transistor.

(b) What type and what concentration of impurities must be implanted to achieve V_T = + 0.6 V and V_T = – 0.6 V ?

SOLUTION :

(a) For unimplanted transistor,

$$\phi_F(substrate) = \frac{kT}{q}\ln\left(\frac{n_i}{N_A}\right) = 0.026\text{V}\cdot\ln\left(\frac{1.45\cdot10^{10}}{4\times10^{18}}\right) = -0.51\text{V}$$

$$\phi_F(gate) = \frac{kT}{q}\ln\left(\frac{N_{D,poly}}{n_i}\right) = 0.026\text{V}\cdot\ln\left(\frac{2\cdot10^{20}}{1.45\times10^{10}}\right) = 0.61\text{V}$$

$$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate) = -0.51\text{V} - 0.61\text{V} = -1.12\text{V}$$

$$Q_{B0} = -\sqrt{2\cdot q\cdot N_A\cdot\varepsilon_{Si}\cdot\left|-2\phi_F(substrate)\right|}$$

$$= -\sqrt{2\cdot1.6\cdot10^{-19}\cdot(4\times10^{18})\cdot11.7\cdot8.85\cdot10^{-14}\cdot\left|-2\cdot0.51\right|}$$

$$= -1.16\cdot10^{-6}\,\text{C/cm}^2$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97\cdot8.85\cdot10^{-14}\,\text{F/cm}}{1.6\cdot10^{-7}\,\text{cm}} = 2.2\cdot10^{-6}\,\text{F/cm}^2$$

$$V_{T0} = \Phi_{GC} - 2\phi_F(substrate) - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$= -1.06 - (-1.12) - (-0.53) - (0.03) = 0.56\text{V}$$

(b) For V_T= 2V;

$$V_T = 2 = V_{T0} - \frac{Q_{II}}{C_{ox}} = 0.56 - \frac{Q_{II}}{C_{ox}}$$

Negative charges needed in this case, so it must be p-type implant in the amount of

$$Q_{II} = qN_I = (V_T - V_{T0})C_{ox}$$

$$N_I = (2-0.56)\times\frac{2.2\times10^{-6}}{1.6\times10^{-19}} = 1.98\times10^{13}\left[cm^{-3}\right]$$

For V_T=-2V, positive charges need, must be n-type implant,

$$N_I = (2+0.56)\times\frac{2.2\times10^{-6}}{1.6\times10^{-19}} = 3.52\times10^{13}\left[cm^{-3}\right]$$

3.12 Using the measured data given, determine the device parameters V_{T0}, k, γ, and λ, assuming $2\phi_F$ = –1.1 V and L=4μm.

V_{GS}(V)	V_{DS} (V)	V_{BS} (V)	I_D(μA)
0.6	0.8	0	8
0.8	0.8	0	59
0.8	0.8	-0.3	37
0.8	1.0	0	60

SOLUTION :

Because the given device is a long channel device, when $V_{DS} \geq V_{GS}$, the transistor operates in s aturation region, therefore

$$I_{DSAT} = \frac{k}{2}\left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right)$$

a) Find λ:

$$\frac{I_{DSAT}\left(Row4\right)}{I_{DSAT}\left(Row2\right)} = \frac{1 + \lambda V_{DS}\left(Row4\right)}{1 + \lambda V_{DS}\left(Row2\right)} = \frac{1+\lambda}{1+0.8\lambda} = \frac{60}{59}$$

$$\lambda = 0.09\left[V^{-1}\right]$$

b) Find V_{T0}:

$$\frac{I_{DSAT}\left(Row2\right)}{I_{DSAT}\left(Row1\right)} = \frac{\left(0.8 - V_{T0}\right)^2}{\left(0.6 - V_{T0}\right)^2}$$

$$V_{T0} = 0.48\text{V}$$

c) Find *k*:
From Row2 data,

$$59 = \frac{k}{2}\left(0.8 - 0.48\right)^2 \left(1 + 0.09 \cdot 0.8\right)$$

$$k = 1.08\left[\text{mA/V}^2\right]$$

d) Find γ:
From Row3 data,

$$37 = \frac{1075}{2}\left(0.8 - V_T(V_{BS} = -0.3)\right)^2 \left(1 + 0.09 \cdot 0.8\right)$$

$$V_T(V_{BS} = -0.3) = 0.55\left[\text{V}\right]$$

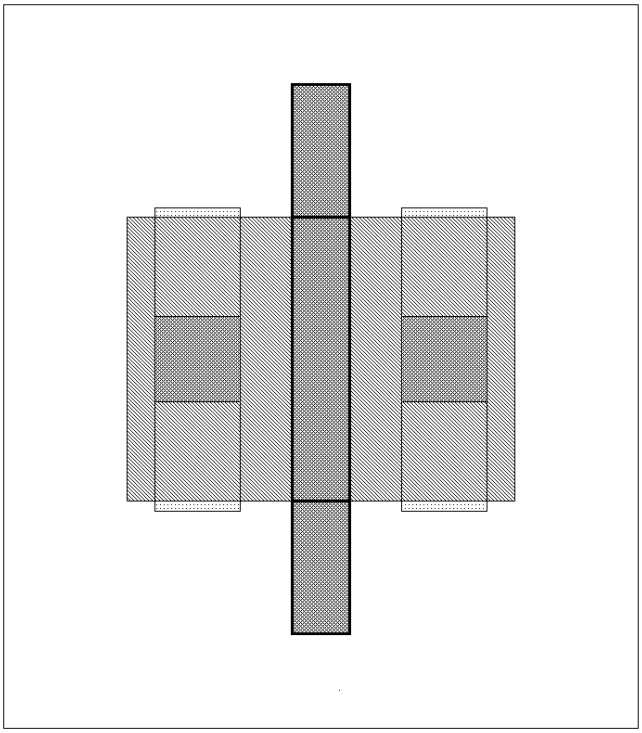
$$0.55 = 0.48 + \gamma\left(\sqrt{0.3 + 1.1} - \sqrt{1.1}\right)$$

$$\gamma = 0.52\left[\text{V}^{1/2}\right]$$

3.13 Using the design rules specified in Chapter 2, sketch a simple layout of an nMOS transistor on grid paper. Use a minimum feature size of 60 nm. Neglect the substrate connection. After you complete the layout, calculate approximate values for C_g, C_{sb}, and C_{db}. The following parameters are given.

Substrate doping $N_A = 4 \cdot 10^{18}$ cm^{-3}
Drain/source doping $N_D = 2 \cdot 10^{20}$ cm^{-3}
W = 300 nm
L = 60 nm
t_{ox} = 1.6 nm
Junction depth = 32 nm
Sidewall doping = $4 \cdot 10^9$ cm^{-3}
Drain bias = 0 V

SOLUTION :



Because the drain bias is equal to 0V, there is no current in the device.
First of all, C_{ox} is calculated like below:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97 \cdot 8.85 \cdot 10^{-14}\,\text{F/cm}}{1.6 \cdot 10^{-7}\,\text{cm}} = 2.2 \cdot 10^{-6}\,\text{F/cm}^2$$

So total gate capacitance Cg is

$$\begin{aligned} C_g &= C_{gb} + C_{gd} + C_{gs} \\ &= C_{ox}WL + C_{ox}WL_D + C_{ox}WL_D \\ &= C_{ox}WL_{(total\ length)} \\ &= 2.2 \cdot 10^{-2}\,\text{F/m}^2 \cdot 300 \cdot 10^{-9}\,\text{m} \cdot 60 \cdot 10^{-9}\,\text{m} \\ &= 0.396\text{fF} \end{aligned}$$

$$\phi_0 = \frac{kT}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^{\,2}}\right) = 0.026\text{V} \cdot \ln\left(\frac{4\times10^{18} \cdot 2\times10^{20}}{2.1\times10^{20}}\right) = 1.11\text{V}$$

$$\phi_{0sw} = \frac{kT}{q} \cdot \ln\left(\frac{N_A(sw) \cdot N_D}{n_i^{\,2}}\right) = 0.026\text{V} \cdot \ln\left(\frac{4\times10^{9} \cdot 2\times10^{20}}{2.1\times10^{20}}\right) = 0.57\text{V}$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\phi_0}}$$

$$= \sqrt{\frac{11.7 \cdot 8.85 \cdot 10^{-14}\,\text{F/cm} \cdot 1.6 \times 10^{-19}}{2} \cdot \left(\frac{4 \times 10^{18} \cdot 2 \times 10^{20}}{4 \times 10^{18} + 2 \times 10^{20}} \right) \cdot \frac{1}{1.11\text{V}}}$$

$$= 54.1 \times 10^{-8}\,\text{F/cm}^2$$

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\phi_0}}$$

$$= \sqrt{\frac{11.7 \cdot 8.85 \cdot 10^{-14}\,\text{F/cm} \cdot 1.6 \times 10^{-19}}{2} \cdot \left(\frac{4 \times 10^{9} \cdot 2 \times 10^{20}}{4 \times 10^{9} + 2 \times 10^{20}} \right) \cdot \frac{1}{0.57\text{V}}}$$

$$= 24.1 \times 10^{-12}\,\text{F/cm}^2$$

The zero-bias sidewall junction capacitance per unit length can also be found as follows.

$$C_{jsw} = C_{j0sw} \cdot x_j = 24.1 \times 10^{-12}\,\text{F/cm}^2 \cdot 32 \times 10^{-7}\,\text{cm} = 77.15\text{aF/cm}$$

The total area of the n^+/p junctions is calculated as the sum of the bottom area and the sidewall area facing the channel region.

$$A = (0.3 \times 0.15)\mu\text{m}^2 + (0.15 \times 0.032)\mu\text{m}^2 = 0.05\mu\text{m}^2$$

$$P = (2 \times 0.3)\,\mu\text{m} + 0.15\mu\text{m} = 0.75\mu\text{m}$$

$$C_{db} = A \cdot C_{j0} + P \cdot C_{jsw}$$

$$= 0.05 \times 10^{-8}\,\text{cm}^2 \cdot 54.1 \times 10^{-8}\,\text{F/cm}^2 + 0.75 \times 10^{-4}\,\text{cm} \cdot 77.2 \times 10^{-18}\,\text{F/cm} = 0.271 \times 10^{-15}\,\text{F}$$

$$= 0.271\text{fF} = C_{sb}$$

3.14 An enhancement-type nMOS transistor has the following parameters:

V_{T0} = 0.48 V
γ = 0.52 $V^{1/2}$
λ = 0.05 V^{-1}
$|2\phi_F|$ = 1.01 V
k' = 168 μA/V^2

(a) When the transistor is biased with V_G = 0.6 V, V_D = 0.22 V, V_S = 0.2 V, and V_B = 0 V, the drain current is I_D = 24μA. Determine *W/L*.

(b) Calculate I_D for V_G = 1 V, V_D = 0.8 V, V_S = 0.4 V, and V_B = 0 V.

(c) If μ_n = 76.3 cm^2/V·s and $C_g = C_{ox} \cdot W \cdot L$ = 1.0 x 10^{-15} F, find *W* and *L*.

SOLUTION :

(a) For enhancement transistor and $V_{T0} > 0$, it must be nMOS.

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right)$$
$$= 0.48 + 0.52 \cdot \left(\sqrt{1.01 + 0.2} - \sqrt{1.01}\right) = 0.529[\mathrm{V}]$$
$$\because V_{DS} = 4 > V_{GS} - V_T = 0.6 - 0.52 = 0.08$$

nMOS transistor is in saturation.

$$\because I_D(sat) = \frac{k}{2}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$
$$\therefore \frac{W}{L} = \frac{2 \cdot I_D(sat)}{k' \cdot \left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right)}$$
$$= \frac{2 \cdot 24 \times 10^{-6}}{168 \times 10^{-6} \times 0.08^2 \times \left(1 + 0.05 \times 0.8\right)} = 42.92$$

(b)

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right)$$
$$= 0.48 + 0.52 \cdot \left(\sqrt{1.01 + 0.4} - \sqrt{1.01}\right) = 0.575[\mathrm{V}]$$
$$\because V_{DS} = 0.02 < V_{GS} - V_T = 0.6 - 0.575 = 0.025$$

nMOS transistor is in linear region.

$$I_D(lin.) = \frac{k'}{2}\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - {V_{DS}}^2\right]\left[1 + \lambda V_{DS}\right]$$
$$= 84 \times 10^{-6} \times 42.92\left[2 \times 0.025 \times 0.02 - 0.02^2\right]\left[1 + 0.05 \times 0.02\right]$$
$$= 2.16[\mu A]$$

(c)

$$C_{ox} = \frac{k'}{\mu_n} = \frac{168 \times 10^{-6}}{76.3} = 2.2 \times 10^{-6}\left[\mathrm{F/cm^2}\right]$$

$$\begin{cases} W \cdot L = \dfrac{C_g}{C_{ox}} = \dfrac{10^{-15}}{2.2 \times 10^{-6}} = 4.5 \times 10^{-8}\left[\mathrm{F/cm^2}\right] \\ \dfrac{W}{L} = 42.92 \end{cases}$$

Solve for W and L,

$$\begin{cases} W = 14.2[\mu m] \\ L = 0.33[\mu m] \end{cases}$$

3.15 An nMOS transistor is fabricated with the following physical parameters:

$N_D = 2.4 \cdot 10^{18}\ \mathrm{cm}^{-3}$

N_A(substrate) = $2.4 \cdot 10^{18}$ cm^{-3}
N_A^+(chan. stop) = 10^{19} cm^{-3}
W =400 nm
Y = 175 nm
L = 60 nm
L_D = 0.01 μm
X_j = 32 nm

(a) Determine the drain diffusion capacitance for V_{DB} = 1.2 V and 0.6 V.
(b) Calculate the overlap capacitance between gate and drain for an oxide thickness of t_{ox} = 18 Å.

SOLUTION :

(a)

$$\phi_0 = \frac{kT}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) = 0.026\text{V} \cdot \ln\left(\frac{2.4\times10^{18} \cdot 2.4\times10^{18}}{2.1\times10^{20}}\right) = 984\left[m\text{V}\right]$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot \frac{1}{\phi_0}}$$

$$= \sqrt{\frac{11.7 \cdot 8.85 \cdot 10^{-14}\text{F/cm} \cdot 1.6\times10^{-19}}{2} \cdot \left(\frac{2.4\times10^{18} \cdot 2.4\times10^{18}}{2.4\times10^{18} + 2.4\times10^{18}}\right) \cdot \frac{1}{984m\text{V}}}$$

$$= 31.8\times10^{-8}\left[\text{F/cm}^2\right]$$

$$A = W \cdot Y + W \cdot X_j = 0.4 \cdot 0.175 + 0.4 \cdot 0.32 = 0.198\left[\mu m^2\right]$$

$$C_j(V) = \frac{A \cdot C_{j0}}{\sqrt{1 - \frac{V}{\phi_0}}}$$

$$C_j(-1.2) = \frac{0.198\times10^{-8} \cdot 31.8\times10^{-8}}{\sqrt{1 + \frac{1.2}{0.984}}} = 0.423\times10^{15}\left[\text{F}\right]$$

$$C_j(-0.6) = \frac{0.198\times10^{-8} \cdot 31.8\times10^{-8}}{\sqrt{1 + \frac{0.6}{0.984}}} = 0.496\times10^{15}\left[\text{F}\right]$$

For sidewall capacitance calculation,

$$\phi_{osw} = \frac{kT}{q} \cdot \ln\left(\frac{N_A(sw) \cdot N_D}{n_i^2}\right) = 0.026\text{V} \cdot \ln\left(\frac{10^{19} \cdot 2.4\times10^{18}}{2.1\times10^{20}}\right) = 1.02\left[\text{V}\right]$$

$$C_{josw}$$
$$= \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A(sw) \cdot N_D}{N_A(sw) + N_D} \right) \cdot \frac{1}{\phi_{osw}}}$$
$$= \sqrt{\frac{11.7 \cdot 8.85 \cdot 10^{-14}\,\mathrm{F/cm} \cdot 1.6 \times 10^{-19}}{2} \cdot \left(\frac{2.4 \times 10^{18} \cdot 10^{19}}{2.4 \times 10^{18} + 10^{19}} \right) \cdot \frac{1}{1.02\mathrm{V}}}$$
$$= 39.6 \times 10^{-8} \left[\mathrm{F/cm^2} \right]$$

$$C_{jsw}(V) = \frac{P \cdot X_j \cdot C_{josw}}{\sqrt{1 - \frac{V}{\phi_{osw}}}} = \frac{(2 \times 175 + 400) \times 10^{-7} \times 32 \times 10^{-7} \times 39.6 \times 10^{-8}}{\sqrt{1 - \frac{V}{\phi_{osw}}}}$$
$$= \frac{1.77 \times 10^{-14}}{\sqrt{1 - \frac{V}{\phi_{osw}}}} [F]$$

$$C_{jsw}(-1.2V) = \frac{1.77 \times 10^{-14}}{\sqrt{1 + \frac{1.2}{1.02}}} = 12 \times 10^{-15} [F]$$

$$C_{jsw}(-0.6V) = \frac{1.77 \times 10^{-14}}{\sqrt{1 + \frac{0.6}{1.02}}} = 14 \times 10^{-15} [F]$$

$$\langle C_{db} \rangle (-1.2V) = C_j(-1.2V) + C_{jsw}(-1.2V) = 0.423 + 12 = 12.423 [fF]$$
$$\langle C_{db} \rangle (-0.6V) = C_j(-0.6V) + C_{jsw}(-0.6V) = 0.496 + 39.6 = 40.096 [fF]$$

(b)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{18 \times 10^{-8}} = 1.92 \times 10^{-6} \left[F / cm^3 \right]$$
$$C_{gd} = C_{ox} \cdot W \cdot L_D = 1.92 \times 10^{-6} \times 400 \times 10^{-7} \times 0.01 \times 10^{-4} = 0.077 [fF]$$